Application No.: 09/438,295 Docket No.: 21737-00013-US

AMENDMENTS TO THE CLAIMS

Claims 1-5 cancelled

6. (Previously amended)A computer readable medium storing program code for causing a computer to write data of bits in a semiconductor device having a plurality of multilevel memory cells, each cell storing at least three levels of data each, comprising:

first program code means f or entering at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, the first and the second data having been coded by a coding method; and

second program code means for arranging the first and the second data bits to store at least a bit of an N-order of the first data bits and at least a bit of an M-order of the second data bits in one of the cells, the N and M being different integral numbers.

7. (Previously amended) The computer readable medium according to claim 6 further comprising:

third program code means for initiating generation of voltages corresponding to the N- and M-order bits; and

fourth program code means for applying the voltage to the one of the cells in response to an address information corresponding to the one of the cells.

Claims 8-25 canceled

26. (Previously amended) A semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, the semiconductor device comprising;

a controller for entering at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, the first and second data having been coded by a coding method; and

a bit data separator for separating the first and second data bits to store at least a bit of an N-order of the first data bits and at least a bit of an M-order of the second data bits in one of the cells, the N and M being different integral numbers.

27. (Previously amended) The semiconductor device according to claim 26, wherein the bit data separator controls the number of bits to be stored in at least one of the cells in accordance with capability of code error correction of the coding method.

28. (Previously amended) The semiconductor device according to claim 26, wherein the bit data separator puts the bits of O number of code data, each code data having a code length P, into positions of arrangement in O lines x P rows and stores the O number of bits in each cell, the O and P being an integral number.

29. (Original) The semiconductor device according to claim 26, wherein the multilevel memory cells are non-volatile semiconductor memories.

30. (Cancelled)

31. (Previously amended) A method of writing at least one code data coded by a coding method in a semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, the method comprising the steps of:

entering at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, the first and second data having been coded by a coding method; and

separating the first and second data bits to store at least a bit of an N-order of the first data bits and at least a bit of an M-order of the second data bits in one of the cells the N and M being different integral numbers.

32. (Original) A computer readable medium storing program code for causing a computer to write at least one code data coded by a coding method in a semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, comprising the program code for dispersing bits constituting the code data over the plurality of multilevel memory cells.

Claims 33-68 canceled